

SEP 27 2004

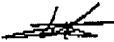
Docket: P910322

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hsu et al.
Serial No.: 10/609,075
Filed: June 27, 2003
For: NON-VOLATILE MEMORY CELL
WITH DIELECTRIC SPACERS
ALONG SIDEWALLS OF A
COMPONENT STACK, AND
METHOD FOR FORMING SAME

Examiner: Nadav, Ori
Group Art Unit: 2811

CERTIFICATE OF FACSIMILE TRANSMISSION
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7722 on September 27, 2004.


Kenton R. Mullins, Reg. No. 36,331

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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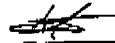
Sir:

Submitted herewith are

- ~ Amendment (9 pages including this Transmittal);
- ~ The Commissioner is hereby authorized to charge any needed fees to deposit account 50-1600.

Respectfully submitted,

Date: September 27, 2004


Kenton R. Mullins
Attorney for Applicant
Reg. No. 36,331

Stout, Uxa, Buyan & Mullins, LLP
4 Venture, Suite 300
Irvine, CA 92618
Telephone: (949) 450-1750
Facsimile: (949) 450-1764

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AMENDMENT

Dear Sir:

This is in response to the non-final Office Action mailed from the United States Patent and Trademark Office on May 28, 2004 in the above-referenced application. An appropriate extension of time is being filed concurrently herewith.

Amendments to the Detailed Description begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks begin on page 7 of this paper.

Application No. 10/609,075

September 24, 2004

Page 2

Docket: P910322

Amendments to the Detailed Description

Please amend the paragraph bridging pages 7 and 8 to read as follows:

Referring to the drawings, FIGS. 2-9B will now be used to describe one embodiment of a method for forming localized trapped charge memory cell structures. FIG. 2 is a cross-sectional view of a semiconductor substrate 120 having an electron trapping structure comprising a first silicon dioxide (oxide) layer 122 formed on an upper surface, a silicon nitride (nitride) layer 124 formed over the first oxide layer 122, and a second oxide layer 126 formed over the nitride layer 124 and a A polycrystalline silicon (polysilicon) layer 128 is formed over the second oxide layer 126.